## AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A memory controller, comprising:

an array of tag address storage locations; and

a command sequencer and serializer unit coupled to the array of tag address storage locations, the command sequencer and serializer unit to control a data cache and an eviction buffer located on at least one memory ~~device~~ module of an off-chip system memory ~~module~~, the memory controller coupled to the memory module via a memory bus, the command sequencer and serializer unit to cause a current line of data to be written from the command sequencer and serializer unit to the data cache, the command sequencer and serializer unit to cause a previous line of data to be evicted out of the data cache to the eviction buffer located on the memory ~~device~~module.

2. (Cancelled)

3. (Currently Amended) The memory controller of claim 1, the command sequencer and serializer to deliver a writeback command to the data cache associated with the memory ~~device,~~ module the writeback command to cause the previous line of data stored in the eviction buffer to be written out to a ~~second memory module~~ memory device of the memory module.

4. (Previously Presented) The memory controller of claim 3, the writeback command including way information and bank address information.

5.-8. (Cancelled)

9. (Currently Amended) A system, comprising:

a processor;

a memory controller coupled to the processor, the memory controller including

an array of tag address storage locations, and

a command sequencer and serializer unit coupled to the array of tag address storage locations; and

an off-chip system memory ~~module~~ coupled to the memory controller, the off-chip system memory including at least two memory modules, each memory module including

at least one memory device, and

a data cache ~~including~~ coupled to an eviction buffer, each coupled to the memory device, the data cache controlled by a plurality of commands delivered by the memory controller, the

memory controller writing a current line of data to the data cache, the memory controller to further instruct the data cache to evict a previous line of data from the data cache into the eviction buffer.

10. (Cancelled)

11. (Previously Presented) The system of claim 9, the memory controller to deliver a writeback command to the data cache, the writeback command to cause the previous line of data to be written out of the eviction buffer to the memory device.

12. (Original) The system of claim 11, the writeback command including way information and bank address information.

13-15. (Cancelled)

16. (New) A memory controller, comprising:

an array of tag address storage locations; and

a command sequencer and serializer unit coupled to the array of tag address storage locations, the command sequencer and serializer unit to control a data cache and an eviction buffer located on at least one memory module of an off-chip system memory, the command sequencer and serializer to deliver a writeback command to the eviction buffer associated with the memory module, the writeback command to cause a previous line of data evicted from the data cache and stored in the eviction buffer, to be written out to a memory device of the memory module.

17. (New) The memory controller of claim 16, wherein the memory controller to issue an eviction signal to the data cache to evict the previous line of data from the data cache into the eviction buffer.

18. (New) The memory controller of claim 16, wherein the memory controller issues the writeback command to cause the previous line of data to be written out of the eviction buffer to the memory device once the memory device is idle.

19. (New) The memory controller of claim 16, wherein the command sequencer and serializer unit to cause a current line of data to be written from the command sequencer and serializer unit to the data cache, the command sequencer and serializer unit to cause the previous line of data to be evicted out of the data cache to the eviction buffer located on the memory module.

20. (New) A memory module, comprising:

at least one memory device; and

a data cache coupled to an eviction buffer, each coupled to the memory device, the data cache controlled by a plurality of commands delivered by a memory controller over a memory bus,

the memory module to receive a writeback command, the writeback command to cause a previous line of data, evicted from the data cache and stored within the eviction buffer, to be written out of the eviction buffer to the memory device.

21. (New) The memory module of claim 20, wherein the data cache to evict the previous line of data from the data cache into the eviction buffer according to an eviction signal received from the memory controller.

22. (New) The memory module of claim 20, wherein the writeback command including way information and bank address information.

23. (New) A system memory comprising:

at least two memory modules, each memory module including:

at least one memory device, and

a data cache coupled to an eviction buffer, each coupled to the memory device.

24. (New) The system memory of claim 23, wherein a memory module to receive a writeback command, the writeback command to cause a previous line of data, evicted from the data cache, to be written out of the eviction buffer to the memory device of the memory module.

25. (New) The system memory of claim 23, wherein a memory module to store a current line of data within a data cache of the memory module, the memory module to evict the previous line of data from the data cache to the eviction buffer located on the memory module in response to a received eviction signal.